BOE

Approval Sheet

■ **Preliminary specification**
☐ **Final specification**

Customer Name	**xxx xxx**
Product Description	**2.1inch 16000RGB*1600 TFT-LCD Module**
Version	**Pre.0**
Supplier	**BOE**
Module Code	VS021XRM-NW0-DKP0

Customer Approval		BOE Approval	
SIGNATURE/TITLE	**DATE**	**SIGNATURE/TITLE**	**DATE**
PREPARED BY		**PREPARED BY**	
_____/_____	_____	_____/_____	_____
REVIEWED BY		**REVIEWED BY**	
_____/_____	_____	_____/_____	_____
APPROVED BY (R&D)		**APPROVED BY (R&D)**	
_____/_____	_____	_____/_____	_____
APPROVED BY (QA)		**APPROVED BY (QA)**	
_____ _/_____	_____	_____ _/_____	_____

ORDOS YUANSHENG
OPTOELECTRONICS TECHNOLOGY CO.,LTD.

Product Specification

Product Name : 2.1" TFT-LCD Module

Model Name : VS021XRM-NW0-DKP0

Description : 2.1" 1600RGB×1600 16.7M Color

PREPARED BY	CHECKED BY	APPROVALED BY

ORDOS YUANSHENG
OPTOELECTRONICS TECHNOLOGY CO.,LTD.

Revision History

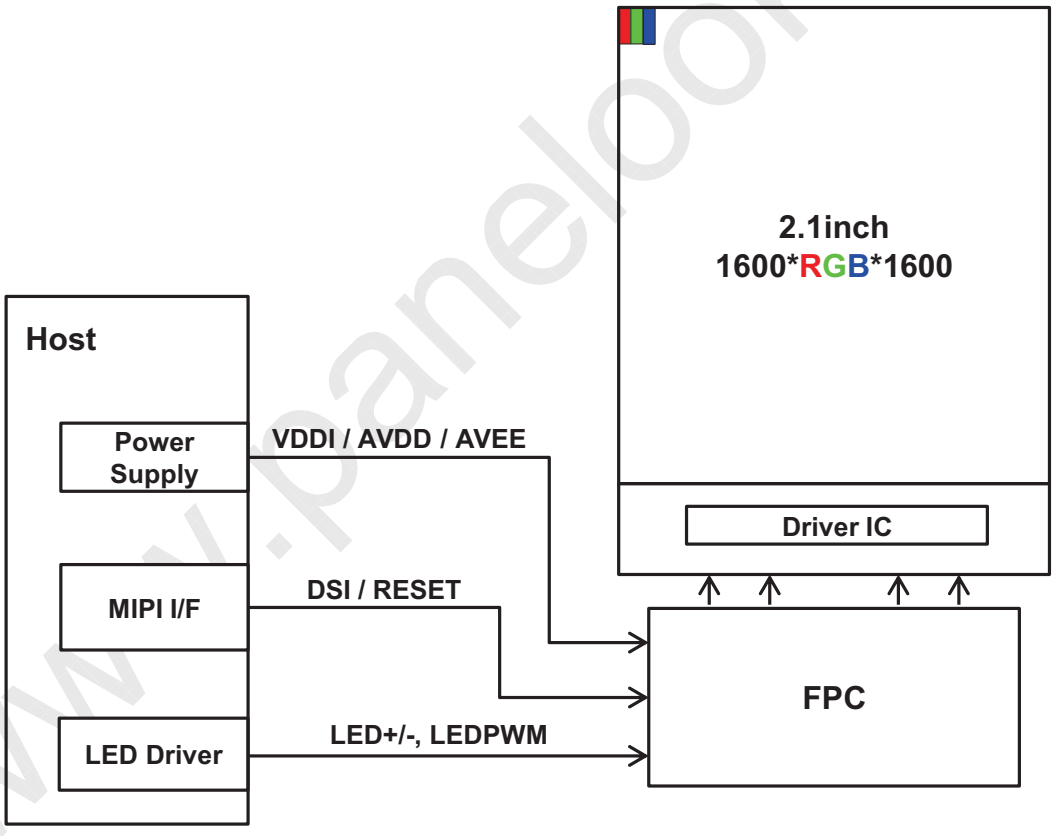
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0	-	Initial Release	2019.10.11	GONG LEI

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

The 2.1inch TFT-LCD Module is a Color Active Matrix TFT LCD panel using LTPS (Low Temperature Poly-silicon) TFT's (Thin Film Transistors) as an active switching devices. This module has a 2.1 inch diagonally measured active area with 1600*1600 resolutions (1600 horizontal by 1600 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- High PPI
- Fast response time
- High frame ratio
- High luminance, low reflection and wide viewing angle
- RoHS、Halogen Free Compliant

1.3 Application

- Virtual Reality Device
- Augmented Reality Device

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Display method	Active matrix TFT		
Display mode	Transmission mode, Normally black		
Screen size	2.1” (38.4mm)	inch	diagonally
Number of pixels	1600(H) × 1600(V)	pixels	1058 ppi
Pixel pitch	8(H) × 24(V)	um	
Pixel arrangement	RGB stripe		
Display colors	16.7M	colors	8bit
NTSC Ratio	70.8%		
LCM Outline Dimension	41.2(H) × 45.3(V) × 1.66 (T)	mm	Note 1)
LCM Weight	6.0 ±1.0	gram	
Driver IC	R63455		
Interface	MIPI DSI (Video Mode)		
Surface Treatment	HC, ≥3H		

Note:

1) Protection film is not included.

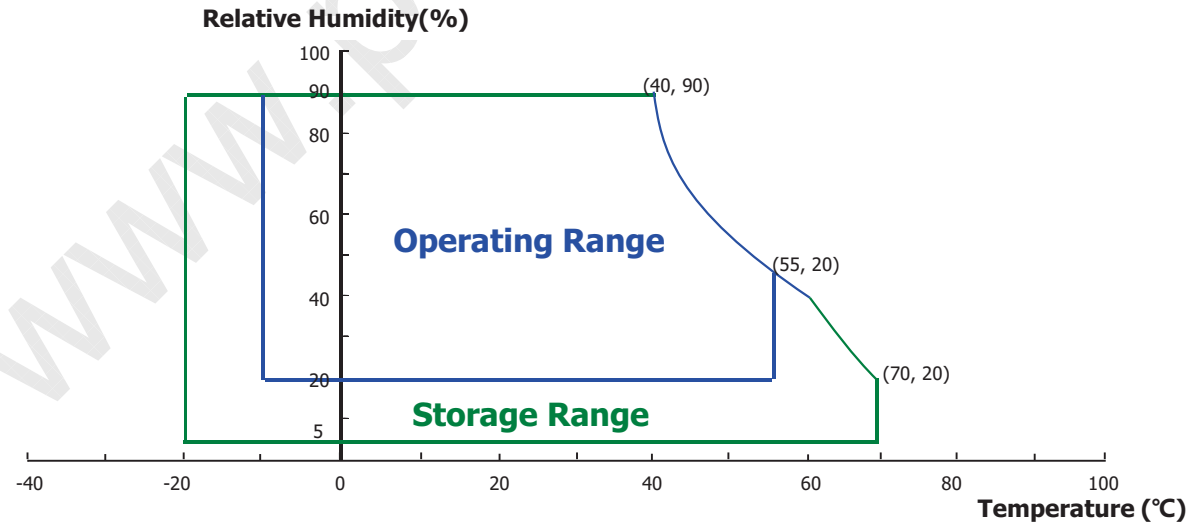
2.0 ABSOLUTE MAXIMUM RATINGS

< Table 2. Absolute Maximum Ratings> [Ta =25±2 ℃]

Items	Symbol	Rating	Unit	Remark
Logic voltage	VDDI	-0.3 to +1.8	V	
Positive Analog Power Supply Voltage	AVDD	-0.3 to +6.0	V	
Negative Analog Power Supply Voltage	AVEE	-6.0 to +0.3	V	
LED forward current	I_{LED}	45	mA	each LED 20% on duty
Storage temperature	T_{STG}	-40 to +70	℃	
Operation temperature	T_{OPR}	-10 to +55	℃	
Humidity (ambient temeprature=Ta)	Ta≤60℃, 90% RH Max.			

Note 1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop. It is not allowed for any of these ratings to be exceeded. Make sure all the design characte ristics are adequate before the panel is initialed.

Note 2: Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Panel

< Table 3. LCD Panel Electrical Specifications > [Ta =25±2 ℃]

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Logic voltage		VDDI	1.7	1.8	1.9	V	Note 1
Positive Analog Power Supply Voltage		AVDD	5.7	6.0	6.3	V	
Negative Analog Power Supply Voltage		AVEE	-6.3	-6.0	-5.7	V	
Frame Ratio		FPS	-	70/90		Hz	
Input signal voltage	High level	V_{IH}	0.7×VDDI	-	VDDI	V	
	Low level	V_{IL}	VSSI	-	0.3×VDDI	V	
Output signal voltage	High level	V_{OH}	0.8×VDDI	-	VDDI		
	Low level	V_{OL}	VSSI	-	0.2×VDDI		
Current consumption		I_{VDDI}	-	79.8	87.7	mA	Note 2
		I_{AVDD}	-	8.7	12	mA	
		I_{AVEE}	-	-5.4	-11	mA	
Driver IC ESD		HBM	- 2	-	+2	kV	
		MM	-200	-	+200	V	

Note 1:
The value can be adjusted by software to optimize display quality.
The operation is guaranteed under the recommended operating conditions only. The oper ation is not guaranteed if a quick voltage change occurs during operation. To prevent nois e, a bypass capacitor must be inserted into the line close to power pin. Please make sure all the design settings are used within this range before the panel is initialed.

Note 2:
Test pattern: All White Display

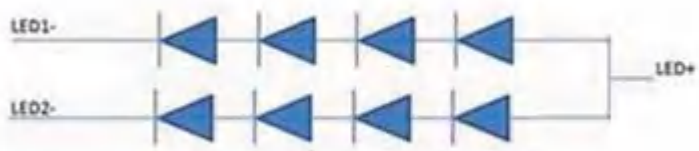
3.2 Back-light Unit

< Table 4. LED Driving Specifications > Ta=25+/-2°C

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Current	If	-	45mA@20%duty	-	mA	Note1
Forward Voltage	Vf	-	6.5	-	V	Note1
Power Consumption	P_{BL}	-	468	-	mW	Note2
LED Q'ty			8		Ea	

Note 1: The driving condition is defined for each LED chip.
Note 2: The B/L power consumption is defined for the backlight module.
the schematic drawing of the backlight unit is as the figure.
The B/L power consumption is based on 20% on duty mode

Ref. Total power consumption(max) depends on LED current/LED driver efficiency, etc.



Back-Light Circuit

4.0 OPTICAL SPECIFICATION

4.1 Overview

The optical characteristics should be measured in a dark room (ambient luminance≤ 1 lux and temperature = 25±2℃) with the equipment of Konica Minolta CA-310 and CS-2000 and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . The center of the measuring spot on the display su rface should stay fixed.

The operation should be under the recommended operating conditions.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	θ_3	CR > 100	-	40	-	degree	Note 1
		θ_9		-	40	-		
	Vertical	θ_{12}		-	40	-		
		θ_6		-	40	-		
Color Gamut (NTSC)			θ = 0°	-	70.8	-	%	
Contrast Ratio		CR	θ = 0°	500	650	-		Note 2
Luminance of White	Center	Y_w	θ = 0°	360	450	-	cd/m^2	Note 3
Luminance Uniformity	5 Points	ΔY5		80%	85%	-		Note 4
Chromaticity (CIE 1931)	Red	Rx	θ = 0°	-	0.640	-		Note 5
		Ry		-	0.330	-		
	Green	Gx		-	0.334	-		
		Gy		-	0.628	-		
	Blue	Bx		-	0.150	-		
		By		-	0.060	-		
	White	Wx		-	0.280	-		
		Wy		-	0.290	-		
Response Time (G to G)		T	θ = 0°	-	-	5.5	ms	Note 6
Flicker			θ = 0°	-	-	-30	db	Note 7
Cross Talk		CT	θ = 0°	-	-	2	%	Note 8

Note 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (FIGURE 1).

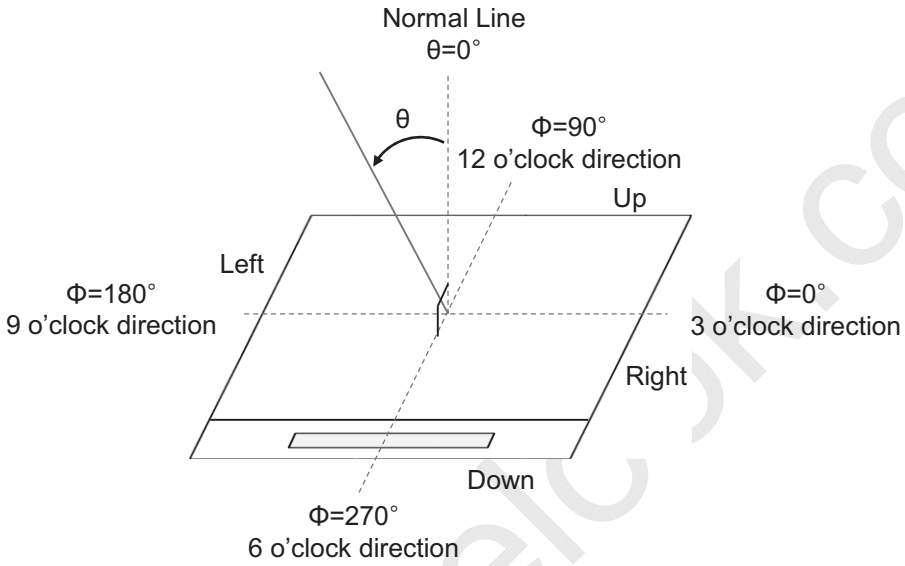


Fig.1 Viewing angle measurement setup

Note 2. Contrast ratio measurements shall be made at viewing angle of θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state (FIGURE 1).
Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 3. Luminance of white is defined as luminance values of the center point across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display. The luminance is measured by CA310 when **the LED current is set at 9mA/ea and the backlight is under the 20% on duty mode.**

Note 4. The White luminance uniformity is then expressed as:
ΔY = Minimum Luminance of 5 points / Maximum Luminance of 5points (FIGURE 3).

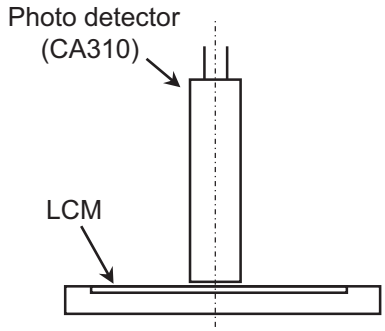


Fig.2 Luminance, uniformity & chromaticity measurement setup

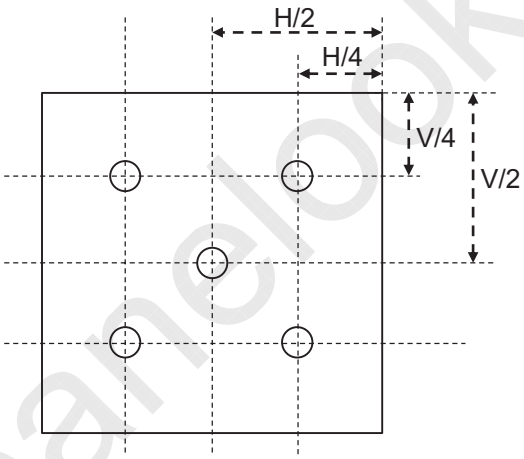


Fig.3 Luminance uniformity measurement setup

Note 5. The color chromaticity is measured with all pixels first in red, green, blue and white. Measurements should be made at the center of the panel.

Note 6. Definition of Response time.
The output signals of photo detector are measured when the input signals are switched between different display pattern (Gray-to-Gray).
The response time is defined as the time interval **between the 10% and 90% of amplitudes** (Fig.4)

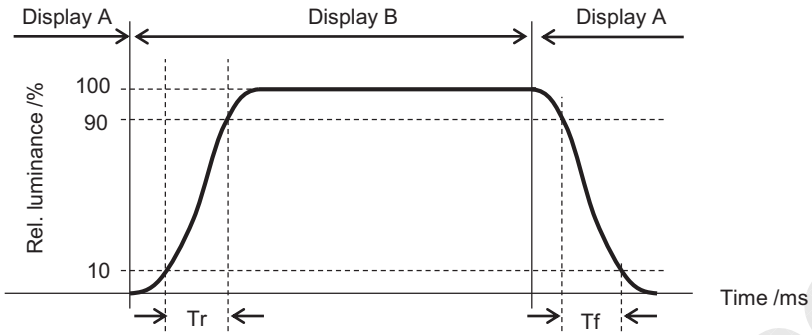


Fig.4 Response Time

Note 7. Flicker

Test equipment: CA310
Test pattern: column inversion (Fig.5)

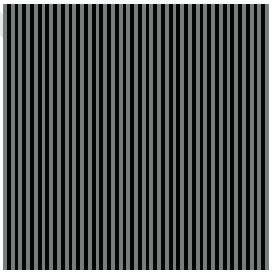


Fig.5 Flicker pattern

Note 8. Cross Talk

Test pattern: Fig.6

$$X - talk = maximum\left(\frac{Y1 - Y1'}{Y1}, \frac{Y2 - Y2'}{Y2}, \frac{Y3 - Y3'}{Y3}, \frac{Y4 - Y4'}{Y4}\right)$$

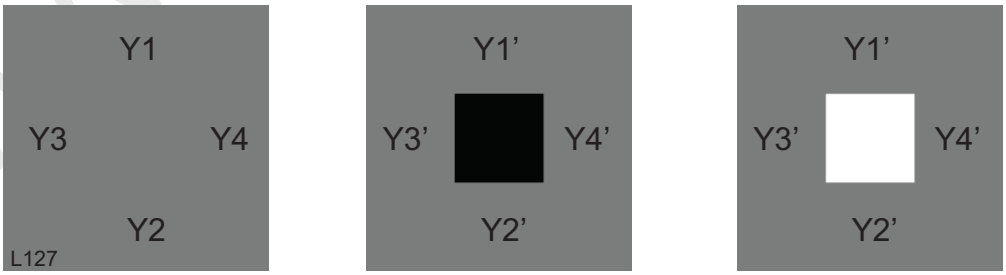


Fig.6 Cross-talk pattern

5.0 INTERFACE CONNECTION

The electronics interface connector is **Kyocera 145863050024829+**
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Connector:145863050024829+					
NO.	**Symbol**	**Description**	**NO.**	**Symbol**	**Description**
1	GND	Ground	**2**	NC	No Connection
3	PNSLV	Main port select	**4**	VSP	Positive power
5	BLUPWM	BLU duty control	**6**	NC	No Connection
7	TE	TE signal output	**8**	VSN	Negative power
9	RESET	DDIC reset signal	**10**	GND	Ground
11	GND	Ground	**12**	DSIB_D3_P	MIPI-DSI-Data lane
13	DSIB_D0_P	MIPI-DSI-Data lane	**14**	DSIB_D3_N	MIPI-DSI-Data lane
15	DSIB_D0_N	MIPI-DSI-Data lane	**16**	GND	Ground
17	GND	Ground	**18**	DSIB_CLK_P	MIPI-DSI-Clock lane
19	DSIB_D1_P	MIPI-DSI-Data lane	**20**	DSIB_CLK_N	MIPI-DSI-Clock lane
21	DSIB_D1_N	MIPI-DSI-Data lane	**22**	GND	Ground
23	GND	Ground	**24**	DSIB_D2_P	MIPI-DSI-Data lane
25	DSIA_D2_N	MIPI-DSI-Data lane	**26**	DSIB_D2_N	MIPI-DSI-Data lane
27	DSIA_D2_P	MIPI-DSI-Data lane	**28**	GND	Ground
29	GND	Ground	**30**	DSIA_D1_N	MIPI-DSI-Data lane
31	DSIA_CLK_N	MIPI-DSI-Clock lane	**32**	DSIA_D1_P	MIPI-DSI-Data lane
33	DSIA_CLK_P	MIPI-DSI-Clock lane	**34**	GND	Ground
35	GND	Ground	**36**	DSIA_D0_N	MIPI-DSI-Data lane
37	DSIA_D3_N	MIPI-DSI-Data lane	**38**	DSIA_D0_P	MIPI-DSI-Data lane
39	DSIA_D3_P	MIPI-DSI-Data lane	**40**	GND	Ground
41	GND	Ground	**42**	NC	No Connection
43	ID0	ID Pin(low : 0)	**44**	LED+	LED Positive power
45	ID1	ID Pin (high : 1)	**46**	NC	No Connection
47	IOVCC1	Power for digital circuit	**48**	LED1-	LED Negative power
49	IOVCC2	Power for digital circuit	**50**	LED2-	LED Negative power

Remark:
Pin 3 “PNSLV” is a Main Port select pin, which is should be connected to the ‘L’ level;

6.0 Block Diagram

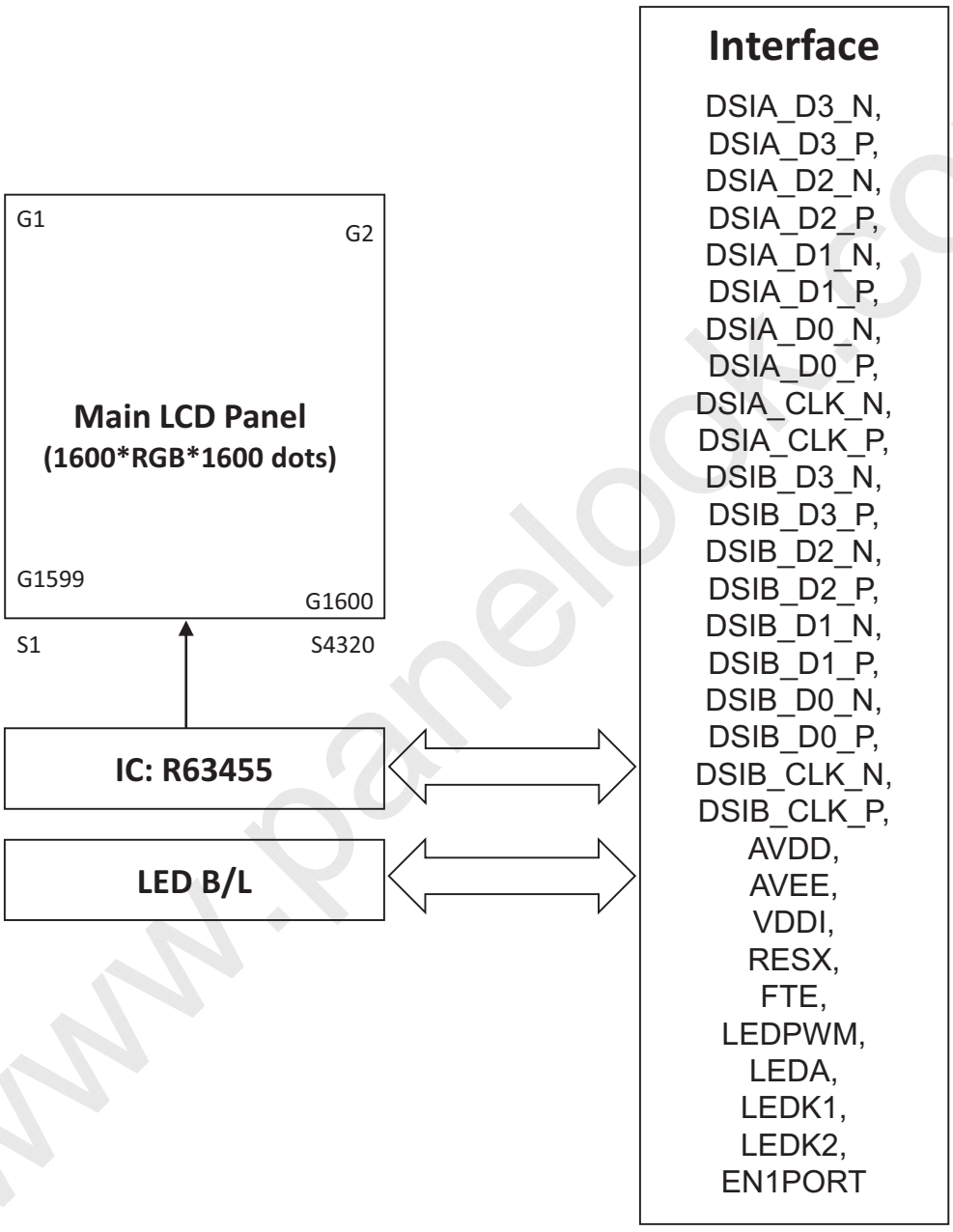
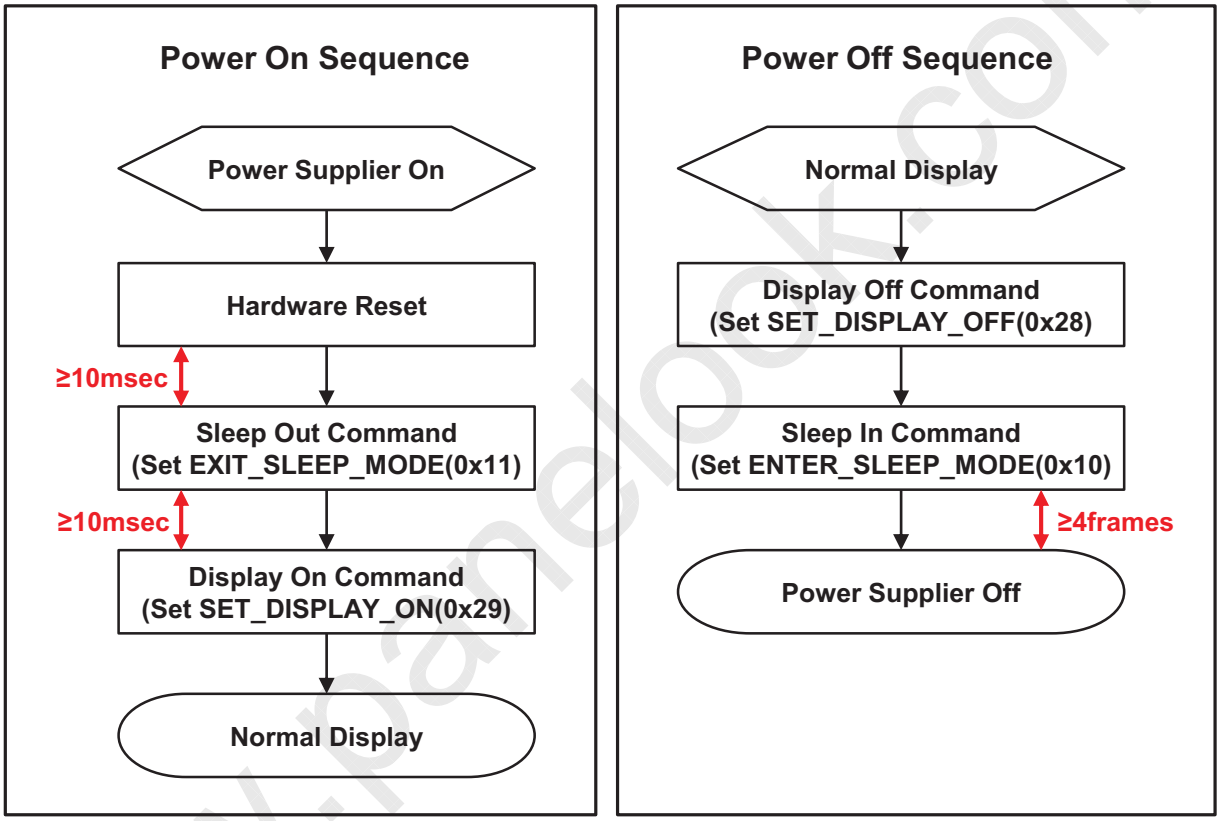


Figure 5. Block diagram

7.0 Timing Characteristics

7.1 Power On/Off Sequence

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



■ **Power On/Off Sequence**

R63455 can be operated by supplying the VSP and VSN power supplies directly.

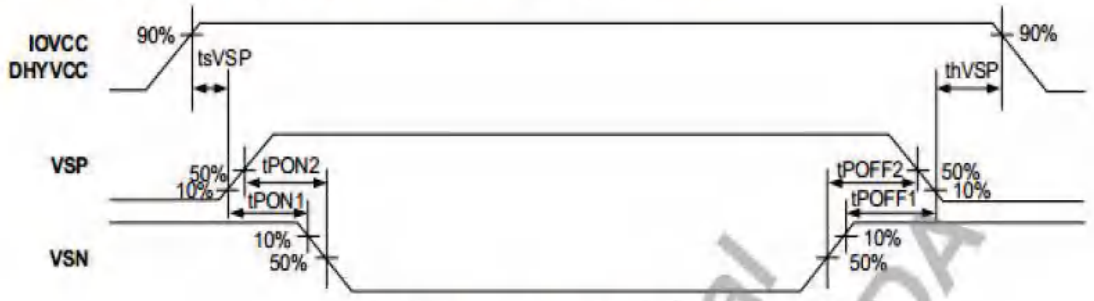


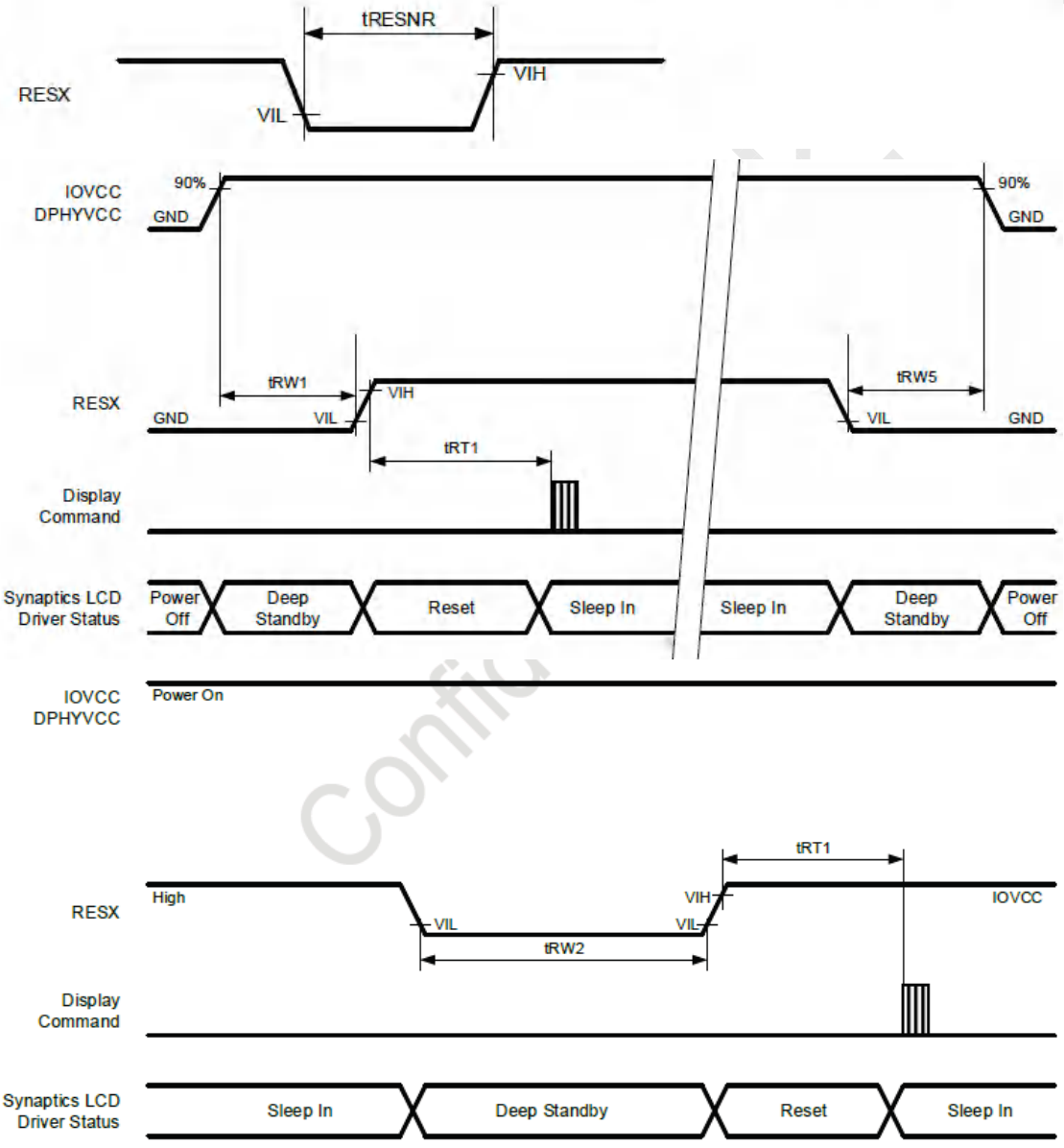
Figure 8. Power supply on/off timing

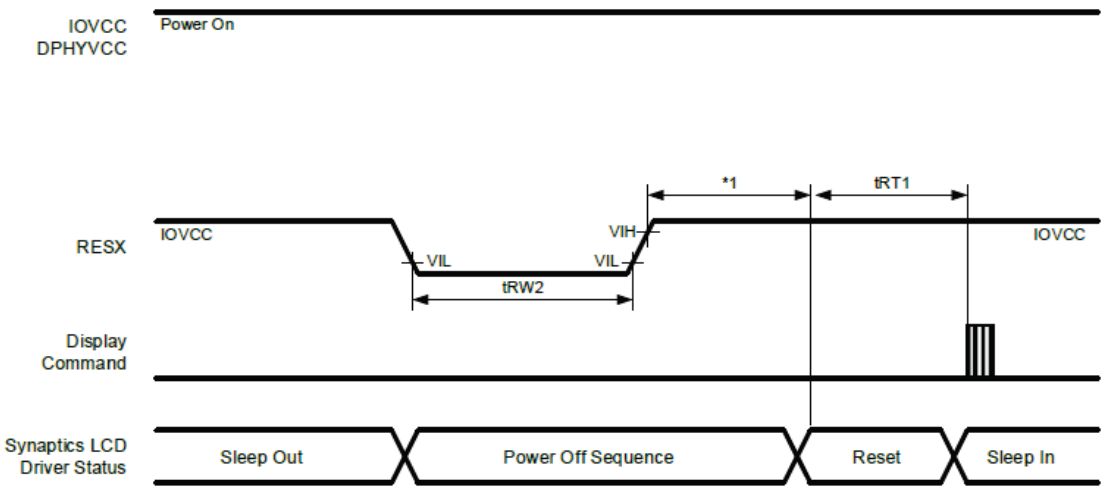
Table 23. Power supply timing specifications

Item	Symbol	Unit	Test Condition	Minimum	Maximum
VSP-VSN delay time (10% to 10%)	tPON1	µs	Power on	0	–
VSP-VSN delay time (50% to 50%)	tPON2	µs	Power on	0	–
System power on to VSP ON time	tsVSP	ms	Power on	1	–
VSN-VSP delay time (10% to 10%)	tPOFF1	µs	Power off	0	–
VSN-VSP delay time (50% to 50%)	tPOFF2	µs	Power off	0	–
VSP OFF to system power OFF time	thVSP	µs	Power off	0	–

7.2 Reset Input Timing

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Reset low-level width1	tRW1	µs	Power supply on	3000	–	–
Reset low-level width2	tRW2	µs	Operation	1000	–	–
Reset low-level width3	tRW5	ms	Power supply off	25	–	
Reset to MIPI command	tRT1	ms	Sleep in	20	–	–
Noise reject width	tRESNR	µs	–	–	–	1





7.3 Deep Standby Mode Timing

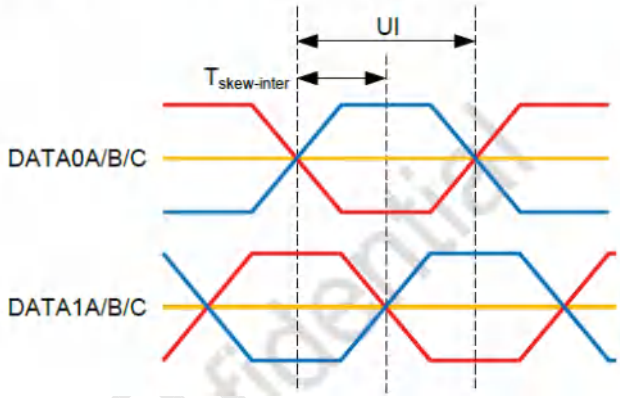
Sequence		Command	State	
			From	To
1	Power on sequence with HWRESET	(RESET_N = Low → High)	Power off	Sleep mode on
2-a	HWRESET	(RESET_N = Low)	–	Deep standby on
2-b	HWRESET sequence	(RESET_N = High -> Low → High)	All status	Sleep mode on
3	exit_sleep_mode sequence	exit_sleep_mode(11h)	Sleep mode on	Sleep mode off (Display off)
5			Sleep mode off (display off)	
6			Sleep mode off (display on)	Sleep mode off (Display on)
7	exit_sleep_mode + set_display_on sequence	exit_sleep_mode(11h) set_display_on(29h)	Sleep mode on	Sleep mode off (Display on)
9	set_display_on sequence	set_display_on(29h)	Sleep mode off (display off)	Sleep mode off (Display on)
10			Sleep mode off (display on)	Sleep mode off (Display on)
11	set_display_off sequence	set_display_off(28h)	Sleep mode off (display on)	Sleep mode off (Display off)
12			Sleep mode off (display off)	Sleep mode off (Display off)
13	enter_sleep_mode sequence	enter_sleep_mode(10h)	Sleep mode off (display off)	Sleep mode on
14			Sleep mode off (Display on)	
15			Sleep mode on	
17	soft_reset sequence	soft_reset(01h)	Sleep mode off (display on)	Sleep mode on
18			Sleep mode off (Display off)	
19			Sleep mode on	
21	Deep standby mode on sequence	(RESET_N = High → Low)	Sleep mode on	Deep standby on
22	Deep standby mode off sequence	(RESET_N = Low → High)	Deep standby on	Sleep mode on

7.4 MIPI Interface Characteristics

MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Symbol rate*	fSYMBOL	Msps	IOVCC = DPHYVCC = 1.65 ~ 1.95V	80	–	1300
UI instantaneous	UI	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	0.77	–	12.5
Data transfer rate*	tDSIR	Mbps	IOVCC = DPHYVCC = 1.65 ~ 1.95V	182	–	2971
Inter lane skew	Tskew-inter	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	-3.5	–	+3.5

* 1 C-PHY data transfer rate is 2.28 times the C-PHY symbol rate.



Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum	Footnote
DSICLK frequency	fDSICLK	MHz	IOVCC = DPHYVCC = 1.65 ~ 1.95V	250	–	650	1
DSICLK cycle time	tCLKP	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1.54	–	4	1
DSI data transfer rate	tDSIR	Mbps	IOVCC = DPHYVCC = 1.65 ~ 1.95V	500	–	1300	1
Data to clock setup time	tSETUP	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦ 1000 Mbps	0.15	–	–	1, 3
		ns		0.15	–	–	1, 2, 3
		UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate > 1000 Mbps	0.2	–	–	1, 3
		ns		0.13	–	–	1, 2, 3
Clock to data hold time	tHOLD	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦ 1000 Mbps	0.15	–	–	1, 3
		ns		0.15	–	–	1, 2, 3
		UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate > 1000 Mbps	0.2	–	–	1, 3
		ns		0.13	–	–	1, 2, 3

1. Minimum 110 mV/-110 mV HS differential swing is required for display data transfer.
2. tSETUP/tHOLD times are measured without HS-TX jitter.
3. Minimum tSETUP/tHOLD Time is 0.15 UI or 0.20 UI. This value may change according to the DSI transfer rate.

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Time to drive LP-000 to prepare for high speed transmission	$T_{3\text{-PREPARE}}$	Ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	38	–	95
Time interval during high speed receiver can receive high speed data starting at the beginning of $t_{3\text{-PREPARE}}$	$T_{3\text{-SETTLE}}$	Ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	95	–	300
Time from driving LP-000 to sending sync word[1]	$T_{3\text{-PREPARE}}$ + $T_{3\text{PREAMBLE}}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	300ns*1	–	-
Time to drive LP-111 after a HS burst	$T_{HS\text{-EXIT}}$	Ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	100	–	–
Time to drive LP-000 after a turnaround request	$T_{TA\text{-GO}}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	4 • T_{LPTX}		
Time that the new transmitter waits after the LP-100 state before transmitting the bridge state (LP-000) during a link turnaround	$T_{TA\text{-SURE}}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1 • T_{LPTX}	–	2 • T_{LPTX}
Time that the new transmitter drives the bridge state (LP-000) after accepting control during a link turnaround	$T_{TA\text{-GET}}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	5 • T_{LPTX}		
Length of any low-power state period	T_{LPX}	Ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	50	–	–
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between the master and slave sides	Ratio T_{LPX}	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	2/3	–	3/2
Time that the transmitter continues sending post words (4444444) after the last associated data lane has transitioned to LP mode[2]	$T_{3\text{-POST}}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	224*2	–	–
Length of the low-power transmitter period	T_{LPTX}	Ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	–	(8/fosc)	–

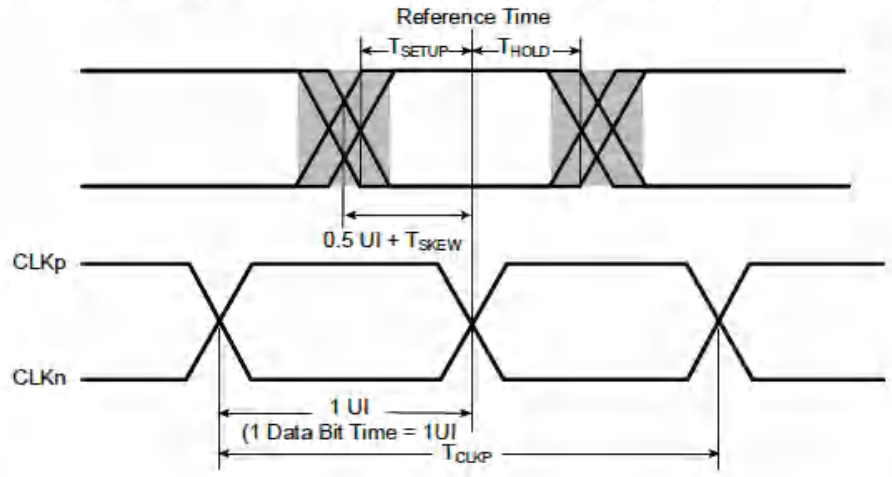
1 The minimum value of $T_{3\text{-PREPARE}}$ is 38 ns and the minimum value of $T_{3\text{-PREAMBLE}}$ is 14 UI, so the minimum value of $T_{3\text{-PREPARE}}$ + $T_{3\text{-PREAMBLE}}$ is calculated as 38 ns + 14 UI. However, there is a relation where $T_{3\text{-PREPARE}}$ + $T_{3\text{-PREAMBLE}}$ > $T_{3\text{-SETTLE}}$. As a result, the minimum value, $T_{3\text{-PREPARE}}$+$T_{3\text{-PREAMBLE}}$, is the same as the $T_{3\text{-SETTLE}}$ minimum value.

2 The minimum value of $T_{3\text{-POST}}$ is defined as 7 UI in the CPHY specification. However, R63455 requires a $T_{3\text{-POST}}$ period at 224 UI. The CPHY specification states that the value of $T_{3\text{-POST}}$ should be adjustable at the transmitter from 7 UI to 224 UI in increments of 7 UI.

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	40 ns + 4 • UI	—	85 ns + 6 • UI
$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	145ns + 10 • UI	—	—
Time to drive flipped differential state after last payload data bit of a HS transmission burst[1, 2]	$T_{HS-TRAIL}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	max (n • 8 • UI, 60 ns + n • 4 • UI)	—	—
Time to drive LP-11 after a HS burst	$T_{HS-EXIT}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	100	—	—
Time to drive LP-00 after a turnaround request	T_{TA-GO}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	4 • T_{LPTX}		
Time that the new TX waits after the LP-10 state before transmitting the bridge state (LP-00) during a link turnaround	$T_{TA-SURE}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1 • T_{LPTX}	—	2 • T_{LPTX}
Time that the new TX drives the bridge state (LP-00) after accepting control during a link turnaround	T_{TA-GET}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	5 • T_{LPTX}		
Length of any low-power state period	T_{LPX}	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	50	—	—
Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between the master and slave sides	Ratio T_{LPX}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	2/3	—	3/2
Time that the transmitter continues sending HS clock after the last associated data lane has transitioned to LP mode[3]	$T_{CLK-POST}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	60 ns + 52 UI	—	—
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting the clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	300	—	—
Time that the HS clock is driven prior to any associated data lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	8	—	—
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	38	—	95
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	60	—	—

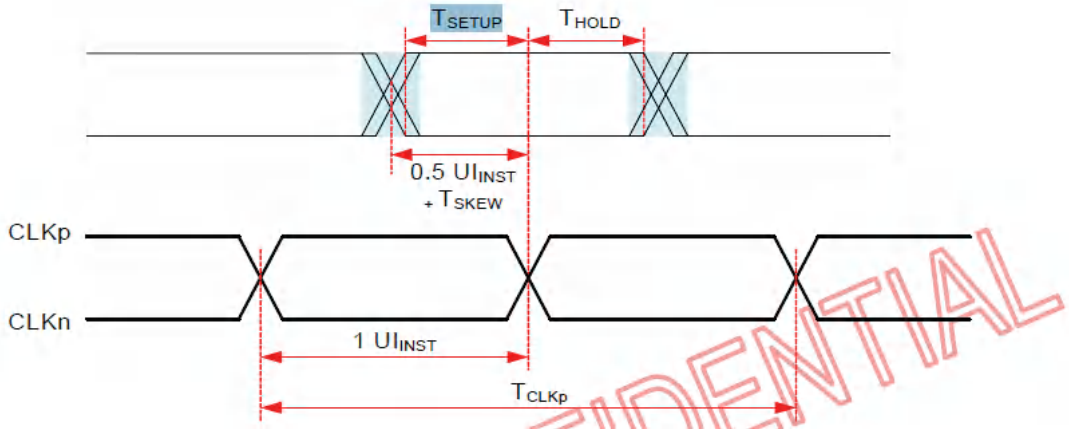
Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Time from the start of THS-TRAIL period to the start of the LP-11 state[2]	T_{EOT}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	—	—	105 ns + n • 12 • UI
Length of the low-power TX period when using the DSI-2 clock[4, 5]	T_{LPTX1}	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	—	1/fTXCLK	—
Length of the low-power TX period when using the internal OSC clock[4, 5]	T_{LPTX2}	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	—	8/fosc	—

1. If a > b then max (a, b) = a, otherwise max (a, b) = b
2. Where n = 1 for forward direction HS mode.
3. R63455 works with this specification, although the last part of the internal process remains when the clock lane enters LP-11 and R63455 works without the remaining process if tCLK-POST is more than 512 UI.
4. R63455 uses the DSI clock from the host processor if the DSI-2 clock lane is active, and uses the internal oscillator clock if the DSI-2 clock lane is stopped.
5. See section "DSI-2 Control Setting (B6h)" (D-PHY) in this document for more information about the DSITXDIV register function.



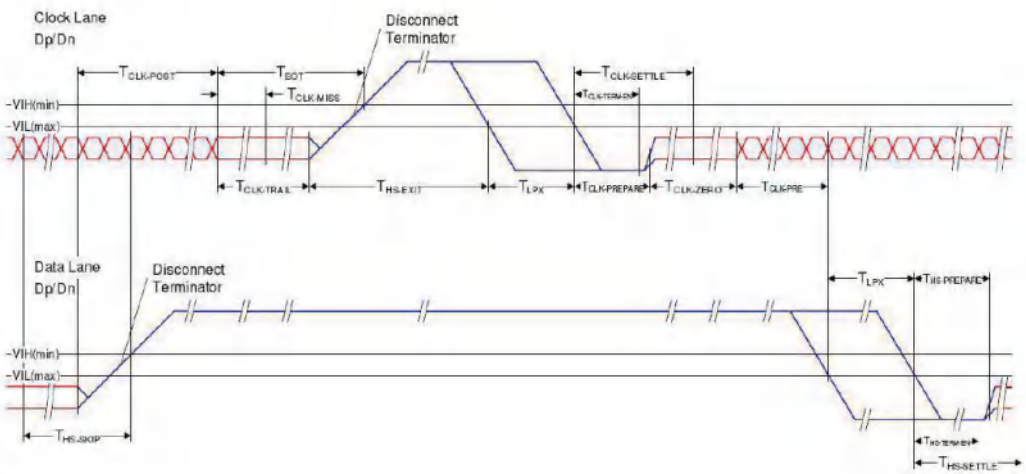
High speed mode

High Speed Data Transmission: Data-Clock Timing

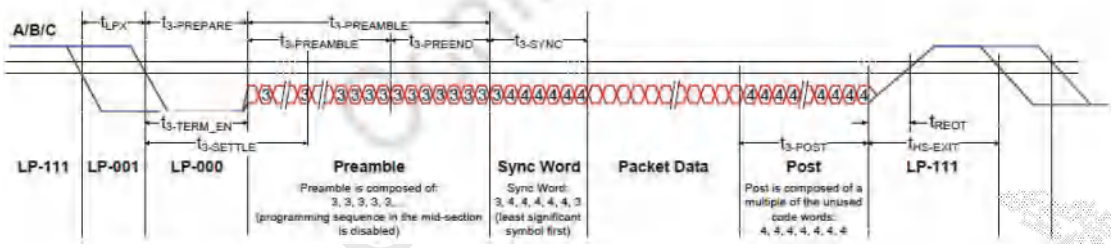


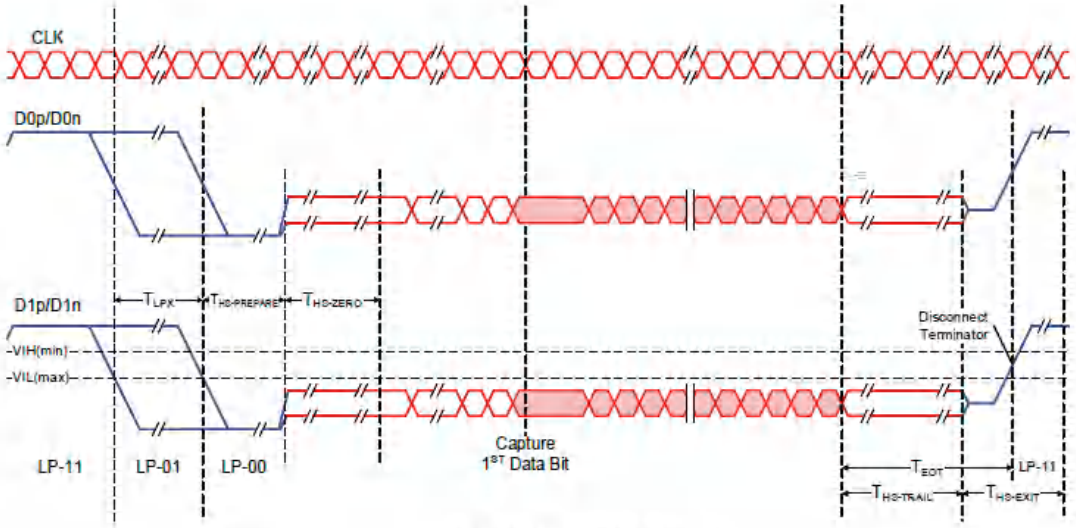
Switching Clock lane

Switching the Clock Lane between Clock Transmission and Low-Power Mode

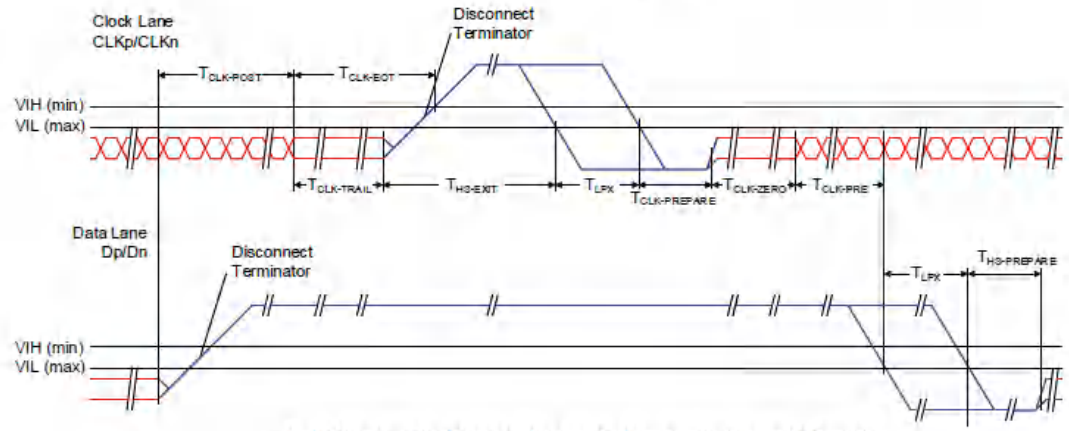


Timing request between data transmission



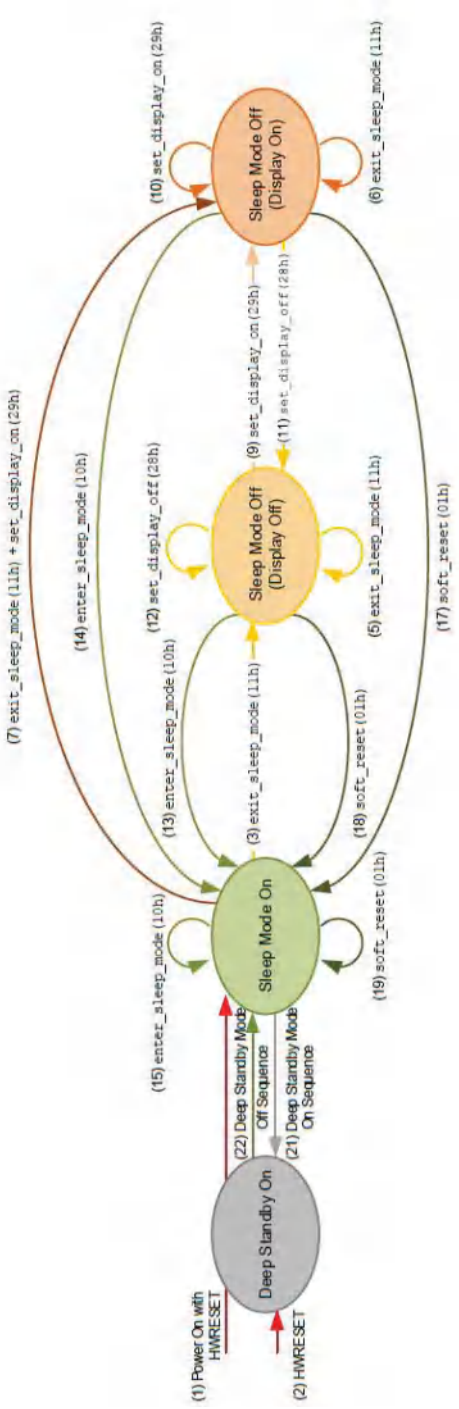


HS data transmission in bursts



Switching the clock lane between clock transmission and LP mode

7.5 Operating Sequence (for reference only)



7.6 Initial Code Setting

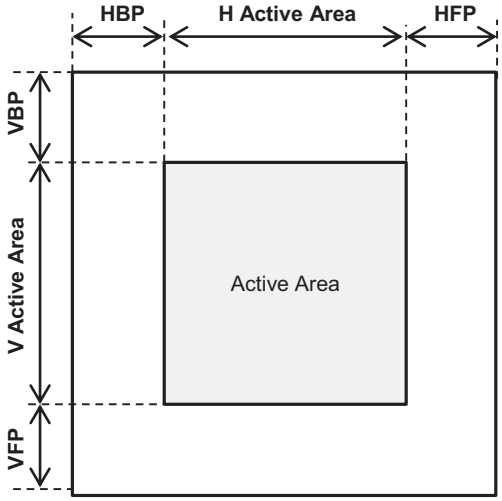
☐ Speed & Porch Setting (for reference only)

Item			Symbol	Min.	Typ.	Max.	Unit
Speed*	Frame Rate		-	-	70/90		Hz
	Line Time		-	-	2.5	-	us
	Dot CLK		-	-	-	-	MHz
	MIPI Speed		-	-	700	-	Mbps
Porch	Horizontal	Horizontal total time	Htotal	-	TBD	-	dot
		Horizontal Active time	Hactive		1600		dot
		Horizontal Pulse Width	Hsync	-	1	-	dot
		Horizontal Back Porch	HBP	-	20	-	dot
		Horizontal Front Porch	HFP	-	30	-	dot
	Vertical	Vertical Total	Vtotal	-	TBD	-	line
		Vertical Active	Vactive		1600		line
		Vertical Pulse Width	Vsync	-	1	-	line
		Vertical Back Porch	VBP	-	29	-	line
		Vertical Front Porch	VFP	-	150	-	line
Lane				-	4	8	Lane

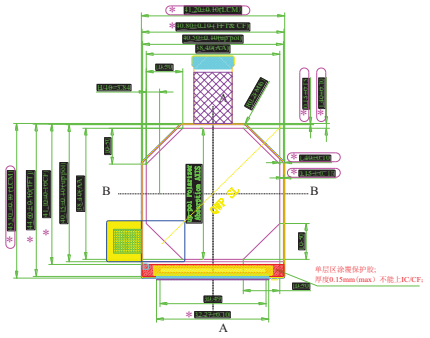
* The Driver IC supports VESA DSC V1.0 and V1.1 Data compression Decoder.

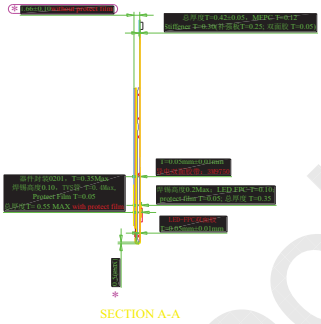
☐ Display Scan Direction

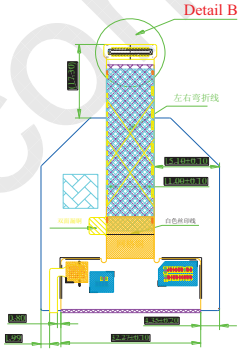
	Data Direction	36h
正向 扫描		00h
反向 扫描		c0h

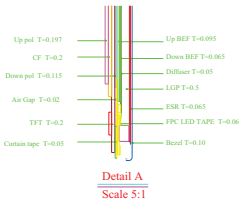


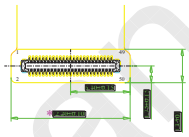
8.0 MECHANICAL CHARACTERISTICS

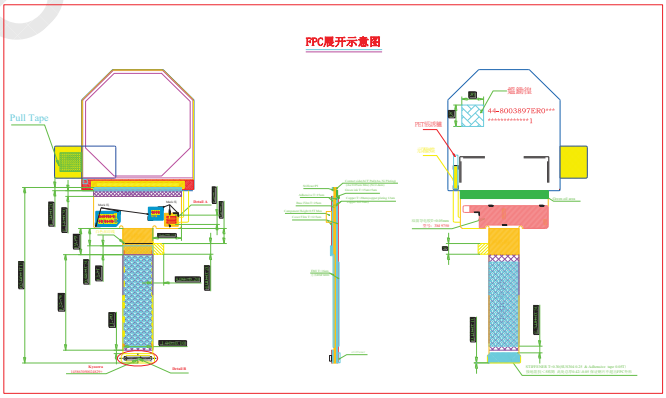












1	Frame	AL2505	1	
1	Back Cover	SUS304	1	0.1
2	REFLECTOR	ESR	1	0.065
3	LGP	TR1501A 0.5注塑	1	0.5
4	DIFFUSER	HBS-247	1	0.05
5	PRISM(D)	TBEF2-DT-LS	1	0.065
6	PRISM(U)	BEF4-DML-LS	1	0.095
7	CURTAIN TAPE	H1350BFU	1	0.05
8	Down pol	LT	1	0.115
9	Glass	CF+TFT	2	0.2+0.2
10	Up pol	LT	1	0.197

9.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 7. Reliability Test Conditions>

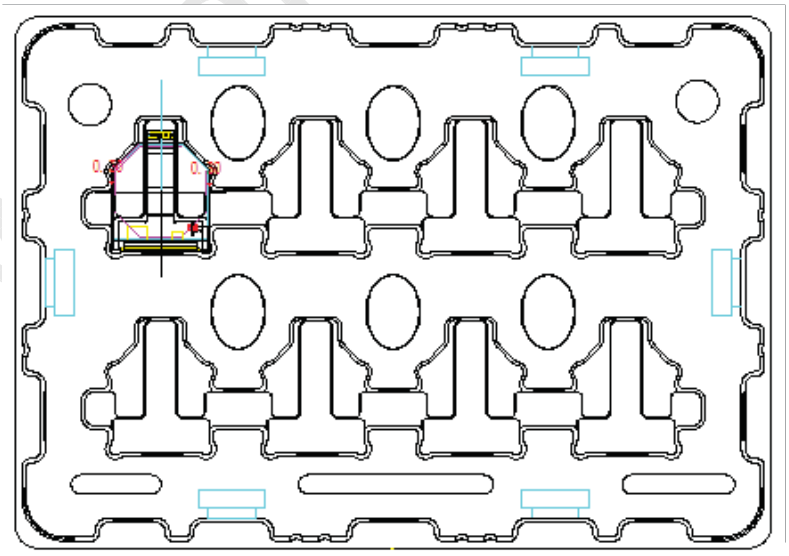
No.	Test Items	Conditions
1	High temperature storage	Ta = 70 ℃, 48 hrs
2	Low temperature storage	Ta = -40℃, 48 hrs
3	High temperature & high humidity operation test	Ta = 60 ℃, 90%RH, 48hrs
4	High temperature operation	Ta = 55 ℃, 48 hrs
5	Low temperature operation	Ta = -10 ℃, 48 hrs

Remark：The Reliability test items can only be applied to the BLU 20% on duty Mode

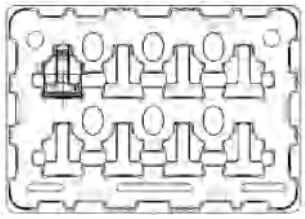
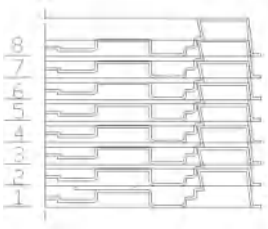
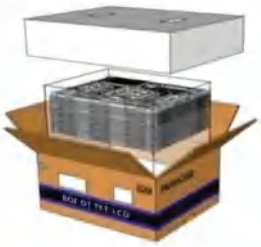
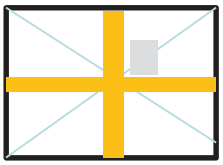
10.0 PACKING INFORMATION

10.1 Packing Description

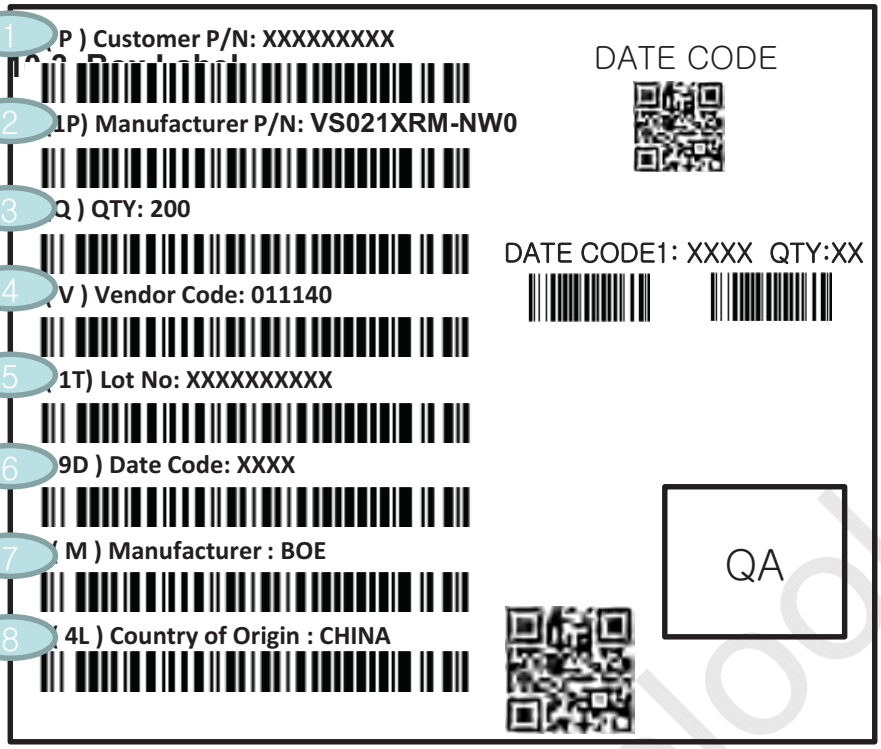
No.	Description	Quantity	Size (mm)
1	LCM per Box	200pcs	
2	LCM per Tray	8pcs	
3	PET Tray	26ea （1ea empty）	320mm ×225mm×16mm
4	Antistatic Bag	1ea	650×550×0.08mm
5	PE Bag	1ea	480(L)×380(W)
6	inner box	1ea	375×280×290mm
7	Out Box	1ea	545(L)×380(W)×270(H)
8	Distribution label		



10.2 Packing Procedure

Put 8pcs LCM into the PET tray ;	Stack the Trays with LCMs in 25 layers，then cover 1 empty tray on the top；200pcs LCM /25Tray	Put the 26 layers of Tray into an electrostatic shielding bag;
 Step 1	 Step 2	 Step 3
Put the Pet bag into the inner box	Put the inner box into the Out Box	Seal the outer box and mark the lable on the surface of outer box. 84pcs LCMs/Box
 Step 4	 Step 5	 Step 6
The 8 cartons are stacked in one layer.They will be stacked in 4 layers		
 Step 7		

BOE	PRODUCT GROUP	REV	ISSUE DATE
	TFT LCD PRODUCT	P1	2019.10.11



Label size :
100mm x80mm*0.08mm

Date code : C922-00041

Instructions:

1. **P/N Code---vendor apply**
2. **FG Code**
3. **Numbers**
4. **Vendor Code**
5. **Box ID**
6. **DATE**
7. **SUPPLIER**
8. **Place of origin**

FG CODE : VS021XRM-NW0-DKP0

Box ID coded rules

serial	1	2	3	4	5	6	7	8	9	10	11	12	13
code	X	X	S	3	1	5	B	0	0	0	1	H	D
Des.	GBN Code		grade	B3	Year		Mon.	Rev	Serial no.(36 decimal, without I,O)				

Year: 2015—15, 2016—16
Month: 1~12→ 1~9, A, B, C