



Product Specification

KADI Model: KD156EWS01NN-DC01-GF

CUSTOMER Model: -

**Description: 15.6” (3840RGB x 2160) AMOLED
Moudle with CTP**

Version: 1.0

KADI	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2024.4.3	2024.4.3	2024.4.3

CUSTOMER APPROVAL	SIGNATURE	DATE



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1. Product Features

- 1) Display color: RGB 10bit/8bit+2FRC/8bit
- 2) Display format: 15.6" (3840RGBx2160)
- 3) Pixel arrangement: Real RGB arrangement
- 4) Interface: eDP 1.4b
- 5) T-con: TBD
- 6) Source IC: RM98110
- 7) Power IC: TBD

2. General Information

Item	Specification	Unit	Note
Outline Dimension	384.16 (H) x 240.09 (V) x 3.1 (D)	mm	
Active area	344.2176 (H) x 193.6224 (V)	mm	
Diagonal size	15.6	inch	
Driver Element	LTPS TFT active matrix		
Display mode	OLED		
Display Colors	RGB 10bit		
Number of pixel	3840*2160(UHD)	Pixel	16:9
Pixel Arrangement	RGB Delta Type		
Pixel pitch	89.64x89.64	µm	
Surface treatment	Anti-Glare		

Note1:Requirements on environmental protection RoHS compliant.

3. Touch Panel Information

Item	Specification
Touch Structure	G+G
Bonding Type with AMOLED	OCA Optical Bonding
Driver IC	ILI2510
Interface	USB
Touch Count Max	10 Points
Surface treatment	AG、AF
Surface hardness	6H
Origin of coordinate	Bottom Right Corner



4. Maximum Rating

Item		Symbol	Min.	Max.	Unit	Note
Storage temperature		TSTG	-40	85	°C	-
Operating temperature		TOPR	-20	70	°C	-
Supply Voltage	System	VCC_3.3V	-0.3	+4.6	V	-
	EL Power	VBAT	-0.3	+24	V	-

5. Electrical Specifications

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
System	Analog/Logic Vol.	VCC_3.3V	-	3.0	3.3	3.6	V	
Panel	Analog Vol.	VBAT	-	8.0	12.0	21.0	V	
Current	Logic	VCC_3.3V	Full white VDD_3.3V=3.3V VBAT=12V	-	420	640	mA	(1)
	Panel	VBAT		-	1100	1370		
Power Consumption	Logic	VCC_3.3V	Full white VDD_3.3V=3.3V VBAT=12V	-	1.4	2.1	W	(1)
	Panel	VBAT		-	13.2	16.4		
Frame Frequency		fps	-	-	60	-	Hz	

Note(1): VCC_3.3V=3.3 (V) VBAT=12.0 (V), Full White pattern, Temperature = 22±3°C Room Temperature

6. Optical Specification

Test condition: 25°C ± 3°C, 65 ± 20%RH, Dark room.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness		Normal (White mode)	352	400	448	cd/m2	(1)
Peak Luminance(10% Box)		VESA HDR		520	-	cd/m2	500TB
Brightness Uniformity		Full white		-	1.4		(2)
Contrast Ratio		Normal $\Theta = \Phi = 0^\circ$	-	100,000	-	-	(3)
Color of CIE Coordinate	White	x	Normal $\Theta = \Phi = 0^\circ$	0.293	0.313	0.333	-
		y		0.309	0.329	0.349	-
	Red	x		0.663	0.683	0.703	-
		y		0.297	0.317	0.337	-
	Green	x		0.195	0.235	0.275	-
		y		0.694	0.734	0.774	-
	Blue	x		0.117	0.137	0.157	-
		y		0.024	0.044	0.064	-
Color Gamut		DCI-P3	98	-100	--	%	(4)
		Adobe	95			%	
		sRGB	100	-	-	%	
White Temperature ° K		Normal $\Theta = \Phi = 0^\circ$	6000	6500	7000	K	
Gamma		Normal $\Theta = \Phi = 0^\circ$	2.0	2.2	2.4	-	(5)
Response time		On/Off	-	1	2	ms	(6)
Viewing Angle		Top/Bottom/Right/ Left CR>10	85		-	°	(7)
Color Shift	Δuv	$\Theta = \Phi = 45^\circ$	-	-	0.025	-	(8)
Image Sticking	ΔL	Macbeth pattern, Max Lum, 3000h, Ambient : ~25°C, Panel : ~45°C	-	-	3.5	%	
Flicker		Normal $\Theta = \Phi = 0^\circ$	-	-	-35	dB	
Crosstalk		Normal $\Theta = \Phi = 0^\circ$	-	-	1.5	%	(9)
TUV blue ray certification		415-455nm/400-500nm			50	%	(10)
OLED Life Time		T50 @ 25°C	15,000	-	-	Hrs	(11)

Note 1: Brightness follows MicroSoft brightness3 (Based on OPR 50%).

The Brightness of full white pattern (OPR100%) is the same as that of OPR 50%.



Note 2: Brightness uniformity

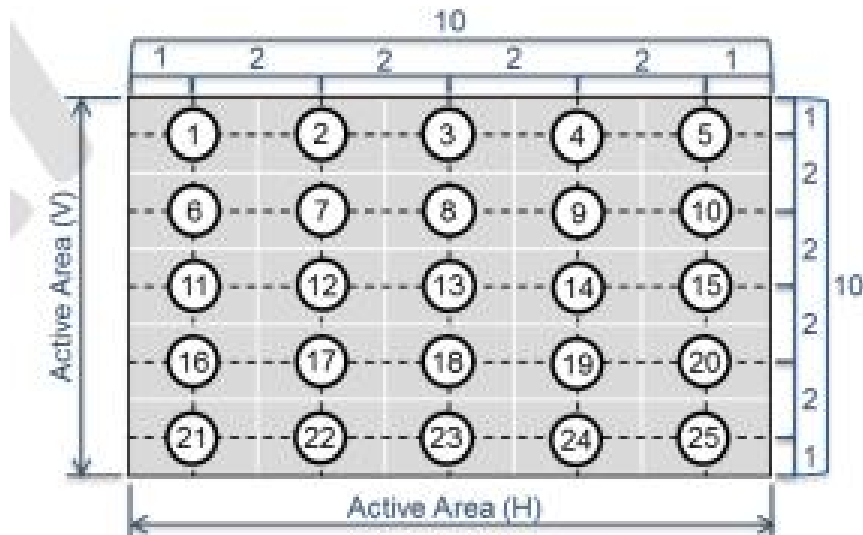
For brightness uniformity measure, EDO's request as below:

1. The test condition is at 25°C and measured on the surface of Display panel module.
2. Measurement equipment: CA310 or similar equipment.
3. The brightness uniformity is calculated by using following formula:

$$\text{Brightness Uniformity} = Bp (\text{Max.}) / Bp (\text{Min.})$$

Bp (Max.) = Maximum brightness in 25 measured spots

Bp (Min.) = Minimum brightness in 25 measured spots.



For 15" or larger

Note 3: Contrast Ratio

Dark Room C.R=LW/LB

LW: full white brightness of display center P0;

LB: full black brightness of display center P0.

Note 4: Color Gamut

For brightness uniformity measure, EDO's request as below:

1. Measurement equipment: CS2000A or similar equipment.
2. DCI-P3 & Adobe color data:

CIE1976	R	G	B
DCI-P3	(0.496,0.526)	(0.099,0.578)	(0.175,0.158)
Adobe	(0.451,0.523)	(0.076,0.576)	(0.175,0.158)
sRGB	(0.451,0.523)	(0.125,0.563)	(0.175,0.158)

3. The color gamut is calculated by using following formula:

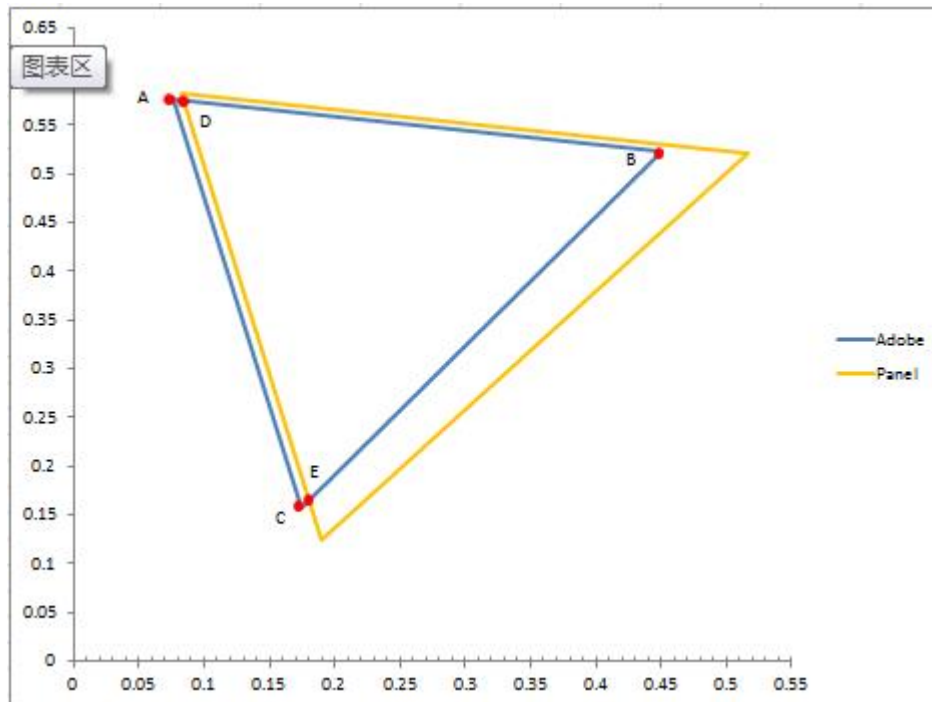
$$\text{Color Gamut \%} = S_{\text{coverage}} / S_{\text{original color gamut}}$$

S_{coverage} : The area covered by panel color gamut

$S_{\text{original color gamut}}$: The triangle area of Adobe or DCI-P3 color gamut

For example:

$$\text{Color Gamut \%} = S_{\text{DEB}} / S_{\text{ABC}} \%$$



Note 5: Gamma

For gamma curve control, EDO's request as below:

1. Calibration the test instrument. Set the screen size parameters, and measure the center point.
2. EDO will test the gray scale below, if possible also can use the patterns of gray 0 to 255 to test: for example:

16, 17, 18, 19, ... , 237, 238, 239,240. Total 225pcs patterns.

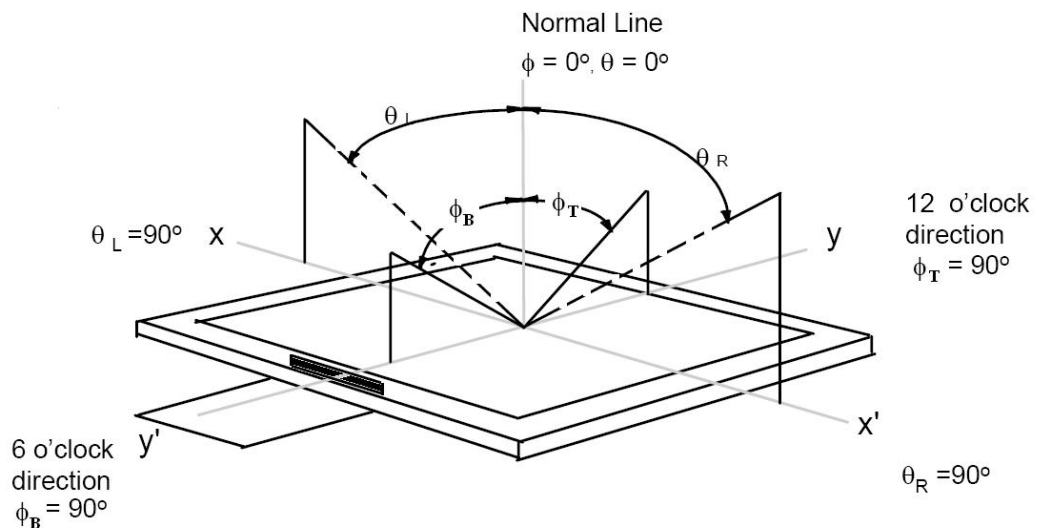
3. Output the measure data. Data number normalization and draw the chart.
4. The whole screen should be complied with the gamma curve of gamma 2.0 or 2.4, it means ± 0.2 error is allowed. But if there are special requirements for the special project, its required specifications can be used as a standard value, please refer the project spec.

Note 6: Response Time

Response time=Pixel turn on and turn off time (White \leftrightarrow Black).
It is measuring transition time from 10% to 90% of luminance.

Note 7: The definition of Viewing Angle

Refer to the graph below marked by θ and ϕ



Note8: Color Shift

For color shift measure:

Fix on white pattern,

On the condition $\theta=0$ $F=0^\circ$, we can get the color coordinate (u_1', v_1') and on $\theta=45^\circ$ $F=45^\circ$ we can get another color coordinate (u_2', v_2')

$\Delta = \text{Square Root}((u_2'-u_1')^2 + (v_2'-v_1')^2)$

JNCD stands for "Just Noticeable Color Difference"

For the (u', v') color space 1 JNCD=0.0040

6.25 JNCD means $\Delta u'v' < 0.0250$.

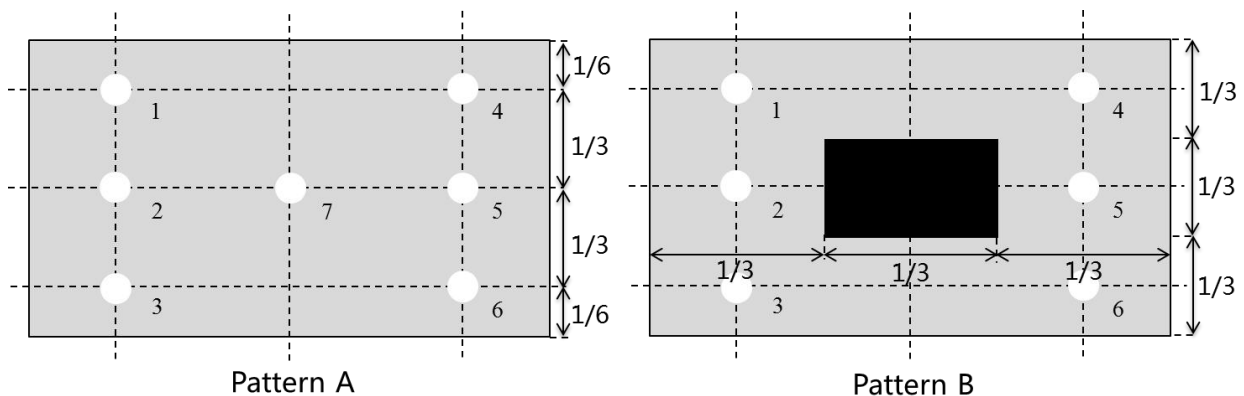
This Requirement is from our customer and we have test some of our phone display and the result is

OK.

Note9: Crosstalk

For crosstalk measure, EDO's request as below:

1. Pattern A and B are of 127 gray, the only difference is that black patch in the middle of pattern B.



2. Calibrate the test instrument.
3. Point 7 in pattern A is used as brightness calibration for each panel. Then measure the brightness of points 1 to 6 in pattern A and B.
4. Calculate the value of crosstalk according to the formula:

$$\text{Crosstalk} = \max\left\{ \frac{\{(B_2-A_2)-[(B_1-A_1)+(B_3-A_3)]/2\}}{A_2}; \frac{\{(B_5-A_5)-[(B_4-A_4)+(B_6-A_6)]/2\}}{A_5} \right\}.$$

Note10: TUV blue ray certification

Under full white mode, test the spectra of center point, and then calculate the intensity in the range 415nm - 455nm and 400nm - 500nm. The ratio of intensity from 415nm - 455nm compared to 400nm - 500nm should be less than 50%.

Note11: OLED Life Time

The test procedure is as follows:

At room temperature(25°C), light the module with typical value brightness(Full white). After that, record the brightness of center point every 24 hours. Then test 600 hours or more to collect the raw data. Finally, use the raw data and the specific formulas to calculate and estimate the T50.



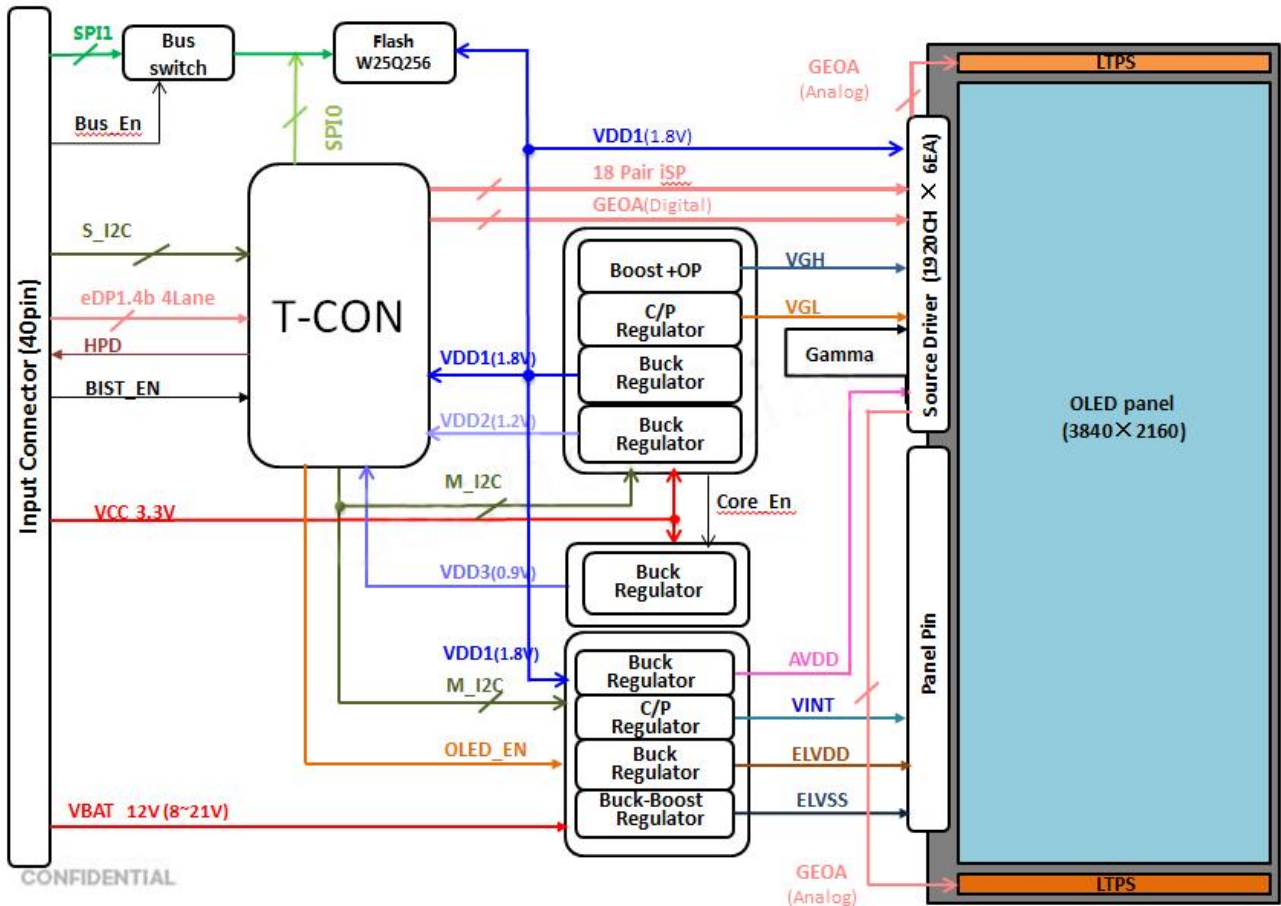
7. I/O connection & Block Diagram

7.1 I/O Connection

Connector Type :20455-040E-66					
Pin #	Signal Name	Signal Description	Pin #	Signal Name	Signal Description
1	NC(HSync)	Do not used. Test pin for display.	21	BIST_EN	BIST enable signal
2	H_GND	High Speed Ground	22	VCC_3.3V	Logic and driver power
3	Lane3_N	Complement Signal Link Lane3	23	VCC_3.3V	Logic and driver power
4	Lane3_P	True Signal Link Lane3	24	VCC_3.3V	Logic and driver power
5	H_GND	High Speed Ground	25	HPD	HPD signal
6	Lane2_N	Complement Signal Link Lane2	26	EN_GND	Ground for EL PMIC
7	Lane2_P	True Signal Link Lane2	27	EN_GND	Ground for EL PMIC
8	H_GND	High Speed Ground	28	NC	NC
9	Lane1_N	Complement Signal Link Lane1	29	VBAT	Power for EL PMIC
10	Lane1_P	True Signal Link Lane1	30	VBAT	Power for EL PMIC
11	H_GND	High Speed Ground	31	VBAT	Power for EL PMIC
12	Lane0_N	Complement Signal Link Lane0	32	NC(EEP_WP)	Do not used. Test pin for display
13	Lane0_P	True Signal Link Lane0	33	NC(MSCL)	Do not used. Test pin for display
14	H_GND	High Speed Ground	34	NC	Do not used. Test pin for display
15	Aux_CH_P	True signal Aux channel	35	NC	Do not used. Test pin for display
16	Aux_CH_N	Complement signal Aux channel	36	NC	Do not used. Test pin for display
17	H_GND	High Speed Ground	37	NC	Do not used. Test pin for display
18	Logic_GND	Logic and driver ground	38	NC	Do not used. Test pin for display
19	Logic_GND	Logic and driver ground	39	NC	Do not used. Test pin for display

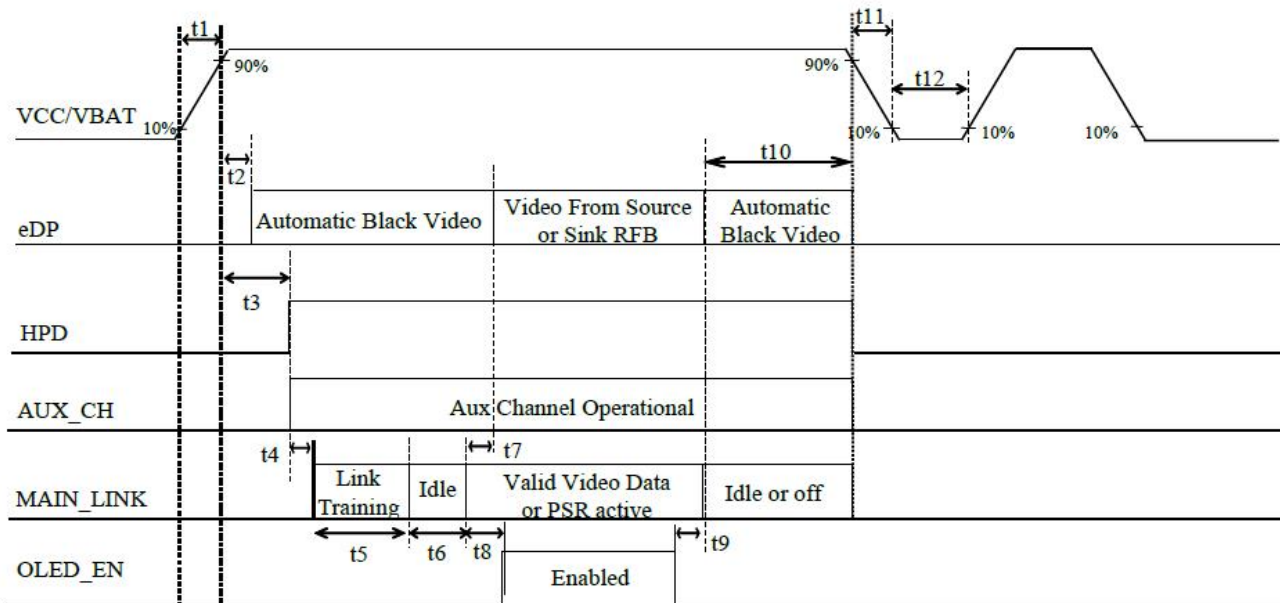
20	Logic_GND	Logic and driver ground	40	NC	Do not used. Test pin for display
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7.2 Display Module Block Diagram



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8. Recommended Operating Sequence



- ◆ It needs minimum 1200ms HPD~Valid Video Data(T4-T6). During the period display back data and valid video data before 1200ms can be lost.
- ◆ Do not keep the interface signal high-impedance or unusual signal when power is on.

Symbol	Min	Max	Unit	Description
t1	0.5	10	ms	Power rail rise time, 10 to 90%
t2	0	200	ms	Delay from VCC/VBAT to automatic Black Video
t3	0	200	ms	Delay from VCC/VBAT to HPD high
t4	-	-	ms	Allows for the Source device to read Link capability
t5	-	-	ms	Link Training duration
t6	-	-	ms	Link idle
t7	0	50	ms	Delay from valid video data from Source to video on display
t8	20	-	ms	Delay from valid video data from Source device to OLED_EN
t9	0	-	ms	Delay from OLED disable to end of valid video data
t10	0	500	ms	Delay from end of valid video data from the Source to power-off
t11	-	10	ms	Power rail fall time, 90 to 10%
t12	500	-	ms	Note

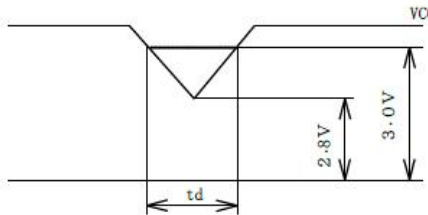
[Note] As for the power off-on sequence for VCC(t12), be sure to keep above mentioned timing. If the VCC power off-on sequence timing is other than shown above, Panel may cause permanent damage.

VCC-dip Condition

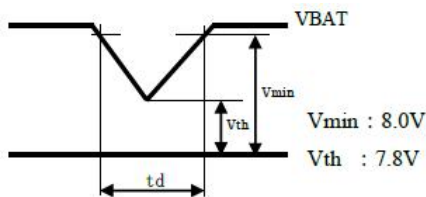
- 1) $2.8V \leq VCC < 3.0V$
 $td \leq 10ms$

Under above condition, the display image should return to an appropriate figure after VCC voltage recovers.

- 2) $VCC < 2.8V$
 VCC-dip conditions should also follow the ON-OFF conditions for supply voltage



VBAT-dip Condition



- 1) $V_{th} \leq V_{BAT} < V_{min} : td \leq 20ms$
 2) $V_{BAT} < V_{th}$: The condition of instantaneous voltage drop is apply to display exception

9. Interface

Resolution	3840(H) × 2160(V)	
eDP Speed	Typ	5.4 Gbps
Frame Freq.	Typ	60 Hz
Porch	HFP + HBP (with HS)	160
	VFP + VBP (with VS)	48

10. Reliability

Item	Condition	Time/Cycle	QTY
High Temperature Operation	70°C	240hrs	5pcs
Low Temperature Operation	-20°C	240hrs	5pcs
High Temperature Storage	85°C	240hrs	5pcs
Low Temperature Storage	-40°C	240hrs	5pcs
High Temperature Humidity Operation	60°C/93%	240hrs	5pcs
Thermal Shock	-40°C/85°C Dwell time=0.5h	100cycles	5pcs
ESD	Operating	Contact +/- 9kV, 150pF, 330Ω, Front 5point	once/point 3pcs
		Air +/- 10kV, 150pF, 330Ω, Front 5point	once/point 3pcs
Vibration test	Non-Operating	1.5Grma 10~500Hz Random X Y Z 1H	1Carton
Packing Drop test	Non-Operating	60cm height, 6-faces, 3-edges and 1-corner(one time for each	1Carton



11. Handling Precautions

- 11.1 When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution.
- 11.2 Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity.
- 11.3 Strong impact & pressure on module and packing is prohibited.
- 11.4 Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display.
- 11.5 Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available.
- 11.6 Image sticking may occur if an image displays for an extended period of time.
- 11.7 When interfered by system's overall mechanical design, an abnormal display may occur.
- 11.8 After considering emitting energy, you should plan your design to satisfy EMI standards.
- 11.9 Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.



13. Packing Specification

TBD

14. The Control of Hazardous substances

The Control of Hazardous substances refer to EDO document 《有害物质管控标准书》
(Standard document for the Control of Hazardous substances) EDO-IS-110,Version 05.